Amendment dated August 18, 2005

Reply to Office Action of April 19, 2005

Amendments to the Claims:

The below listing of claims will replace all prior versions, and listings, of claims in the

application:

**Listing of Claims:** 

1. (Original) A current selective D flip-flop circuit on a chip for receiving at least two

currents and performing biasing current selection, comprising:

a D flip-flop;

a first receiving means having a first receiving means input terminal for receiving one of

at least two currents and having a first receiving means output terminal for providing a first

current, the first current being dependent on the one of at least two currents;

a second receiving means having a second receiving means input terminal for receiving

another of the at least two currents and having a second receiving means output terminal for

providing the second current, the second current being dependent on the another of the at least

two currents;

a summing node to which a first receiving means output terminal is connected to the

second receiving means output terminal for summing the first current and the second current to

obtain a summed current therefrom; and

a current comparator having a current comparator input terminal connected to the

summing node, wherein the current comparator is coupled to the second receiving means for

comparing the summed current with the second current to thereby select one of the first current

and the second current as an output current for biasing the D flip-flop, and the one of the at least

two current is receivable from an on-chip biasing current source and the other of the one of the at

least two current is receivable from a constant biasing source.

2. (Currently Amended) The biasing current selective D flip-flop circuit of claim 1,

wherein the current selector circuit is coupled to the D flip-flop through a current multiplier,

wherein the current multiplier comprises:

a current mirror source being coupled to the current selector circuit; and

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a multiple-output current mirror being coupled to the current mirror source and the D

flip-flop.

3. (Currently Amended) The biasing current selector selective D flip-flop circuit of claim 1,

wherein the first receiving means comprises a first current mirror.

4. (Currently Amended) The biasing current selector selective D flip-flop circuit of claim 3,

the first current mirror comprising at least two PMOS transistors.

5. (Currently Amended) The biasing current selector selective D flip-flop circuit of claim 1

3, wherein the second receiving means comprises a second current mirror.

6. (Currently Amended) The biasing current selector selective D flip-flop circuit of claim 5,

the second current mirror comprising at least two NMOS transistors, and the second receiving

means output terminal being connected to the first receiving means output terminal.

7. (Currently Amended) The biasing current selector selective D flip-flop circuit of claim 4

5, the current comparator comprising:

a third current mirror connected to the drain of a transistor to form an output node,

wherein the output node is connected to an output terminal for providing the output current to the

D flip-flop through the a current multiplier.

8. (Currently Amended) The biasing current selector selective D flip-flop circuit of claim 7,

the third current mirror comprising:

a current comparator input terminal connected to the summing node; and

at least two NMOS transistors.

9. (Currently Amended) The biasing current selector selective D flip-flop circuit of claim 4

3, wherein a voltage supply is connected to the first current mirror.

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10. (Currently Amended) The biasing current selector selective D flip-flop circuit of claim 1,

wherein the second receiving means and the current comparator is connected to ground.

11. (Currently Amended) The biasing current selector selective D flip-flop circuit of claim 1,

the output current being selected by the current comparator from one of the first current and

second current having a larger current magnitude.

12. (Currently Amended) A method for performing biasing current selection in a current

selective D flip-flop circuit, the method comprising the steps of:

applying a first and a second current to a first receiving means input terminal of a first

receiving means and a second current to a second receiving means input terminal of a second

receiving means respectively;

providing the first current from a first receiving means output terminal of the first

receiving means;

providing the second current from a second receiving means output terminal of the

second receiving means;

summing the first current and the second current to produce a summed current at a

summing node;

comparing the summed current with the second current by a current comparator; and

selecting one of the first current and the second current as an output current by the current

comparator in response to the summed current and the second current being compared.

13. (Original) The method of claim 12, the step of providing a first current from a first

receiving means output terminal comprising the step of providing the first current from the first

receiving means having at least two PMOS transistors.

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14. (Original) The method of claim 12, the step of providing a second current from a second

receiving means output terminal comprising the step of providing the second current from the

second receiving means output terminal with the second receiving means output terminal being

connected to the first receiving means output terminal.

15. (Original) The method of claim 12, the step of comparing the summed current with the

second current by a current comparator comprising the step of:

providing the current comparator having a third current mirror connected to the drain of a

transistor to form an output node, wherein the output node is connected to an output terminal for

providing the output current thereat to the D flip-flop.

16. (Original) The method of claim 15, the step of providing the current comparator having a

third current mirror comprising the steps of:

providing the current comparator having a third current mirror comprising:

a current comparator input terminal connected to the summing node for receiving

the summed current thereat; and

at least two NMOS transistors.

17. (Original) The method of claim 12, the step of providing the first current from a first

receiving means output terminal comprising the step of:

providing the first receiving means with a voltage supply connected thereto.

18. (Original) The method of claim 12, the step of providing the second current from a

second receiving means output terminal comprising the step of:

providing the second receiving means and the current comparator with a connection to

ground.

19. (Original) The method of claim 12, the step of comparing the summed current with the

second current by a current comparator comprising the step of:

comparing the current magnitude of each of the summed current and the second current.

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20. (Original) The method of claim 19, the step of selecting one of the first current and the

second current as an output current comprising the step of:

selecting one of the first current and second current having a larger current magnitude.

21. (Currently Amended) A current selective D flip-flop circuit capable of performing

biasing current selection, the current selective D flip-flop circuit comprising:

a D flip-flop;

a current selector circuit current multiplier coupled to the D flip-flop; and

a current multiplier; biasing current selector circuit coupled to the current multiplier,

wherein the eurrent selector circuit is coupled to the D flip flop through the current

multiplier biasing current selector circuit provides at least two input terminals for receiving at

least two biasing currents for selecting one of the at least two biasing currents for biasing the D

flip-flop.

22. (Original) The current selective D flip-flop circuit of claim 21, wherein the current

multiplier comprises:

a current mirror source being coupled to the current selector circuit; and

a multiple-output current mirror being coupled to the current mirror source and the D

flip-flop.